Shashank Karkada Holla

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ACADEMIC QUALIFICATION

Georgia Institute of Technology, Atlanta, Georgia May 2023
Masters in Electrical and Computer Engineering (ECE)
Relevant course work: Computer Architecture, Digital Systems Test, Physical Design Automation, Interconnection Networks.
GPA: 4.0/4.0

R V College of Engineering (RVCE), Bengaluru, India July 2021
Bachelor of Engineering (Electronics and Communication Engineering)
Relevant course work: Digital VLSI Design, Low Power VLSI, Digital Circuit Design
GPA: 9.52/10

EXPERIENCE

Analog Devices Bangalore, India
Engineering Intern Feb 2021 – July 2021
- Worked on Digital Fault Injection(DFI) process on an ASIC for Battery Management System (BMS).
- Understood and implemented the flow for managing the DFI process using commercially available solutions.
- Designed 6 tests and workflow for SPI block of the System on Chip (SOC) to achieve 96% coverage.
- Documented the workflow and wrote scripts to ease DFI setup bringup.

Analog Devices Bangalore, India
Applications Design Intern Jun 2020 – Aug 2020
- Implemented digital FIR and IIR filters using MATLAB and SystemVerilog
- Designed test benches and verified performance metrics like frequency cut off, gain, Signal to Noise ratio (SNR).
- Automated the characterization of these filters using Python to generate inputs and visualize outputs dynamically.

Team Chimera (Formula SAE team), R V College of Engineering Bangalore, India
Safety Circuits and Information Systems Engineer Aug 2018 – May 2021
- Worked on circuit-level designing, prototyping, and testing of circuits like brake system plausibility device and insulation monitoring device that enhance driver safety in electric cars.
- Managed a group of 5 as a part of the safety circuits sub system. Served as the Electrical Systems Officer (ESO) at Formula Bharat 2020.
- Developed the driver information system on the dashboard by using PHYTEC, an ARM based Single Board Linux Computer to communicate between Kelly Motor Controller and LinearTech BMS using CAN protocol.
- Participated in the 2019 and 2020 editions of Formula Bharat, a national level engineering design competition held.

Indian Institute of Science (IISc) Bangalore, India
Research Intern Jun 2019 – July 2019
- Worked on the self-driving car project by IISc and Wipro (WIRIN) in a team of four. Implemented a RaspberryPi and Arduino based system to collect sensor data and visualize it in real-time for the ADAS.
- Developed a data acquisition system that collects data from various physiological sensor signal such as ECG, PPG, Heart rate sensor. Synchronized data collection from various sources using NTP and optimized data transmission between controllers and sensors.

SKILLS

Programming: C, C++, Python, Javascript, Android Development
Hardware Description Languages: Verilog, SystemVerilog
VLSI & Circuit Design: Eagle PCB, Proteus, Cadence Virtuoso, Cadence Xcelium
Microcontrollers used: Arduino, ESP32, Raspberry Pi, Phytec Mira

PROJECTS

Title: Optimised Test Vector reordering for an FSM Feb 2021 – May 2021

- Description: Designed an adaptive Low Power TPG and Optimized ORA for an FSM based Power On Self Test
- Individual Role: Worked on implementing adaptive test vector reordering based on A* algorithm to implement the test pattern generator in Python. Used iVerilog and BooM to implement a 16 stage FSM as a test circuit to verify the adaptive reordering method that optimises coverage and reduces transitions. Achieved 94% fault coverage on the test circuit.
- Document about FSM design: https://jusst.org/wp-content/uploads/2021/06/Design-of-a-Start-Up-Sequence-Controller-for-a-Mammography-Machine.pdf

Title: Development of FPGA Based Image Filtering for medical application Feb 2020 – Apr 2020

- Description: Optimized real-time image filtering process on FPGA by improving data acquisition process and implemented matrix operations on the image in an efficient way in a team of 2. The output was compared for quality and speed with different implementations.
- Publication: Sowmya K.B., Rakshak Udupa T.S., **Holla S.K.** (2021) Implementation of an FPGA Real-Time Configurable System for Enhancement of Lung and Heart Images. In: Khelassi A., Estrela V.V. (eds) Advances in Multidisciplinary Medical Technologies - Engineering, Modeling and Findings. Springer, Cham. https://doi.org/10.1007/978-3-030-57552-6_13

Title: Simulate Out-of-Order Pipelined processor Aug 2021 – Sept 2021

- Description: Simulated 5 stage pipeline processor in C++. Simulation of data forwarding at memory and execute stages to reduce stalls due to RAW hazards was done. Gshare branch predictor was simulated to study the stalls caused due to misprediction. In the second part of the project, Out of Order processors using reorder buffers was simulated.

ACHIEVEMENTS

- Co-presented a paper titled 'Optical fiber communication using an open source expEyes-17 device' which was awarded as the 'Best Paper' at the "International Conference on Multidisciplinary Technologies and Challenges in Industry – 4.0" conference (August 2020)
- Secured second place in maze-solving robot building challenge, 'E-yantra' robotics conducted by Indian Institute of Technology, Bombay (May 2020), amongst more than 1000 teams from all over India .
- Won first place in Infineon Hackathon, held at Infineon Campus, Bengaluru in a team of 4 after optimising an encryption system on an embedded system (December 2019)
- Team's idea of designing a driver assistance system by identifying a distracted driver was selected as top 4 ideas at Smart India Hackathon, conducted by Govt. of India. which was implemented in an overnight hackathon. (March 2019)

CERTIFICATIONS

- 'Computer Architecture' (Nov 2020), 'Algorithmic Toolbox' (May 2020), Coursera,
- 'Neural networks and Deep Learning', Coursera (June 2019)
- 'Embedded System Design with ARM', NPTEL (Mar 2019)
- 'Introduction to probability and Statistics' and 'Cloud Computing', NPTEL (Sep 2018)