Shashank Karkada Holla

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EDUCATION

Georgia Institute of Technology, Atlanta, Georgia Aug 2021 - May 2023
Master of Science in Electrical and Computer Engineering (ECE), GPA: 4.0/4.0

R V College of Engineering (RVCE), Bengaluru, India Aug 2017 - July 2021
Bachelor of Engineering in Electronics and Communication Engineering, GPA: 9.52/10

SKILLS

Programming: C, C++, Python, Verilog, SystemVerilog, Javascript, Android Development
VLSI & Circuit Design: Eagle PCB, Proteus, Verdi, iVerilog, yosys
Relevant Coursework: Computer Architecture, Digital Systems Test, Physical Design Automation, Interconnection Networks, Digital VLSI Design, Low Power VLSI, Digital Circuit Design

EXPERIENCE

NVIDIA Santa Clara, CA (USA)
ASIC Design Engineer 12 June 2023 – Present
- Worked on the RTL design of ARM architecture based processors.
- Implemented various features using Verilog in the out of order scheduler pipeline block and the pipeline execute block.
- Improved power consumption of the processor by using techniques such as clock gating, data gating and optimised architecture. Involved in improving timing of various paths using techniques such as pipelining, suggesting improvments to the architecture.
- Involved in debugging functional bugs using Synopsys Verdi. Understand ARM assembly language to debug tests.
- Involved in architecture discussions, improving verification infrastructure through scripting.
- Wrote concise documentation to help with knowledge transfer and understanding.

Meta Platforms Sunnyvale, CA
Silicon Physical Design Intern 29 Aug 2022 – 2 Dec 2022
- Worked on optimizing placement of cells based on hints from RTL. Involved in Python based RTL code generation project for ML accelerators.
- Integrating new placement flow to the RTL build generation to help designers decide placement of certain logic. Saw improvement of 1% to 5% in Average power consumption.

NVIDIA Santa Clara, CA
ASIC Design Intern, CPU (Remote) 31 May 2022 – 19 Aug 2022
- Implemented RTL features in Decode stage of CPU related to multithreading and instruction decode.
- Worked on automating global flows tasks using Perl, Makepp and Bash scripts.
- Developed scripts that use REST APIs to connect to internal bug tracking and documentation service to update reports and the history of tests.

Analog Devices Bangalore, India
Engineering Intern Feb 2021 – July 2021
- Worked on Digital Fault Injection(DFI) process on an ASIC for Battery Management System (BMS).
- Implemented the flow for managing the DFI process using commercially available solutions.
- Designed 6 tests and workflow for SPI block of the System on Chip (SOC) to achieve 96% coverage.
- Documented the workflow and wrote scripts to ease DFI setup bringup.

PROJECTS

Title: Smart Charging systems for EV Jan 2022 – Feb 2023

- Designed an embedded system, cloud server and mobile app to control charging of Electric Vehicles. Hardware support for Level 1 and Level 2 EV charging. Implemented algorithm to optimize charging to save cost, environment and time.
- K. V. Sastry, S. Holla, S. Tater, et. al, "Development and Demonstration of a Smart Charging System for Plug-in Electric Vehicles," IEEE Transportation Electrification Conference & Expo, 2023.
- Patent - Electric vehicle smart charging algorithms and hardware

Title: On chip network traffic visualizer for Garnet(GEM5) March 2022 – Apr 2022

- Developed a Python based network visualizer to analyze traffic bottlenecks and link usage for on chip networks from the data extracted from Garnet2.0. Presented at GEM5 workshop 2022.

Title: Simulating Out-of-Order Pipelined processor Aug 2021 – Sept 2021

- Simulated 5 stage pipeline out of order processor using reorder buffers in C++. Simulated data forwarding at memory and execute stages to reduce stalls due to RAW hazards. Gshare branch predictor was simulated to study the stalls caused due to misprediction.

Title: Optimised Test Vector reordering for an FSM Feb 2021 – May 2021

- Designed an adaptive Low Power TPG and Optimized ORA for an FSM based Power On Self Test. Worked on implementing adaptive test vector reordering based on A* algorithm to implement the test pattern generator in Python. Achieved 94% fault coverage on the test circuit.
- Document about FSM design: https://jusst.org/wp-content/uploads/2021/06/Design-of-a-Start-Up-Sequence-Controller-for-a-Mammography-Machine.pdf

Title: Development of FPGA Based Image Filtering for medical application Feb 2020 – Apr 2020

- Optimized real-time image filtering process on FPGA by improving data acquisition process and implemented matrix operations on the image efficiently, in a team of 2.
- Publication: Sowmya K.B., Rakshak Udupa T.S., **Holla S.K.** (2021) Implementation of an FPGA Real-Time Configurable System for Enhancement of Lung and Heart Images. In: Khelassi A., Estrela V.V. (eds) Advances in Multidisciplinary Medical Technologies - Engineering, Modeling and Findings. Springer, Cham. https://doi.org/10.1007/978-3-030-57552-6_13

ACHIEVEMENTS

- Secured first place in Qualcomm Best Engineering Award in Georgia Tech Hack for building an app and a system to optimize electricity consumption, (Atlanta 2022)
- Secured second place in maze-solving robot building challenge, 'E-yantra' robotics conducted by Indian Institute of Technology, Bombay (May 2020), amongst over 1000 teams from all over India.
- Won first place in Infineon Hackathon, held at Infineon Campus, Bengaluru in a team of 4 after optimising an encryption system on an embedded system (December 2019)

PUBLICATIONS

[1] John Mamish, Rawan Alharbi, Sougata Sen, Shashank Holla, Panchami Kamath, Yaman Sangar, Nabil Alshurafa, and Josiah Hester. "NIR-sighted: A Programmable Streaming Architecture for Low-Energy Human-Centric Vision Applications". In: *ACM Transactions on Embedded Computing Systems* (2024).

[2] Kartik V Sastry, Shashank Holla, Shreyas Tater, Eric Gustafson, David G Taylor, and Michael J Leamy. "Design and demonstration of a smart charging system for plug-in electric vehicles". In: *2023 IEEE Transportation Electrification Conference & Expo (ITEC)*. IEEE. 2023, pp. 1–6.

[3] KB Sowmya, TS Rakshak Udupa, and Shashank K Holla. "Implementation of an FPGA Real-Time Configurable System for Enhancement of Lung and Heart Images". In: *Advances in Multidisciplinary Medical Technologies Engineering, Modeling and Findings: Proceedings of the ICHSMT 2019*. Springer International Publishing. 2021, pp. 199–213.